Scalable arrays of rf Paul traps in degenerate Si

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We report techniques for the fabrication of multizone linear radio frequency Paul traps that exploit the machinability and electrical conductivity of degenerate silicon. The approach was tested by trapping and laser cooling $^{24}Mg^{+}$ ions in the two following trap geometries: a single-zone two-layer trap and a multizone surface-electrode trap. From the measured ion motional heating rate we determine an electric field spectral density at the ion's position of approximately 1×10^{-10} $(\mathrm{V/m})^2 \cdot \mathrm{Hz}^{-1}$ at $\omega_z/2\pi = 1.125$ MHz when the ion lies 40 μm above the trap surface. One application of these devices is controlled manipulation of atomic ion qubits, the basis of one form of quantum information processing. [doi:10.1063/1.3254188]

Much recent ion trap research is motivated by the goal of building a useful quantum information processor (QIP) using trapped atomic ions as qubits (two-level quantum systems). In one approach, chains of laser-cooled ions are confined in linear radio frequency (rf) Paul traps with segmented trap electrodes.[1–4] Although the theoretical and experimental groundwork has been laid for a large-scale processor, so far only simple traps utilizing up to eight ions have been demonstrated.[2,3,5] Useful qubit computations could be performed using segmented electrodes which define an array of interconnected traps capable of holding and manipulating a large number of ions.[1]

Building such devices poses several microfabrication challenges. For example, the rf potentials (typically 100 to 500 V, $\Omega_{RF}/2\pi = 10$ to 100 MHz) needed for trapping suggest use of a low-loss substrate such as sapphire to prevent heating. However, such materials are incompatible with many through-wafer via technologies needed to distribute potentials to hundreds of control electrodes.[2,6] Also, in vacuum, exposed dielectrics (e.g., the substrate) can accumulate charge giving rise to unwanted stray fields at the ions' location. High aspect-ratio electrodes can mitigate this problem but are difficult to fabricate for our target electrode width of ~ 10 μm. It is desirable that the ratio of electrode height to interelectrode distance ratio be greater than two.[2]

We used degenerate silicon as an electrode material[7] and deep reactive ion etching to build structures that meet these objectives (Figs. 1 and 2). The Si was doped so that the number of electrons in its conduction band approaches that of a metal. In one device (Fig. 2) ions were trapped above the surface of a photolithographically patterned silicon-on-insulator (SOI) heterostructure. Compared with manually assembled traps, this approach reduces alignment errors.[8,9]

The devices were characterized by use of trapped and laser-cooled atomic $^{24}Mg^{+}$ ions. We measured the rate at which ions gain kinetic energy from noisy ambient electric fields, an important characteristic for QIP.[3,10] Also, we obtain reasonable agreement between simulation of the trap potentials and experimentally measured frequencies, important for reliable transport of ions between zones.[2,9]

The suitability of degenerate silicon as a trap electrode material was demonstrated by building and testing multiple ion traps. Two of these traps are discussed in this letter; see also Britton *et al.*[11,12]

Figure 1 shows a single-zone two-layer anodically bonded trap that used a 7070 borosilicate glass as a dielectric spacer (0.06 loss tangent at 1 MHz).[7,11,12] The device was built to demonstrate trapping using semiconducting trap electrodes; prior traps at NIST with similar a geometry used metal electrodes.[8] The silicon was doped by the manufacturer with boron to give it a resistivity of $0.5-1 \times 10^{-3}$ $\Omega \cdot$cm. After the trap electrode pattern was etched,

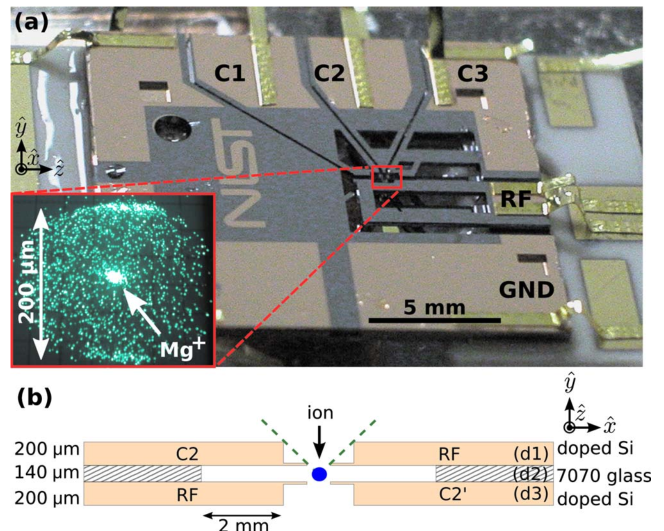

FIG. 1. (Color online) (a) Photograph of a two-layer silicon ion trap with a single trapping zone. The structure consists of two layers of silicon anodically bonded via a glass spacer. Inset: Fluorescence from a single laser-cooled $^{24}Mg^{+}$ ion imaged onto a camera (viewed from above). (b) The chip geometry in cross-section near the trapping region (indicated by a dot); not to scale. The interelectrode spacing was ~ 6 μm (e.g., between C_1 and C_2 near the ion). The ion-electrode distance was ~ 122 μm (e.g., the closest distance between C_2 and the ion). The primed electrodes are not visible in the photograph. The two-tiered etch of the silicon trap electrodes permits a large solid angle for efficient collection of ion fluorescence (dashed lines).

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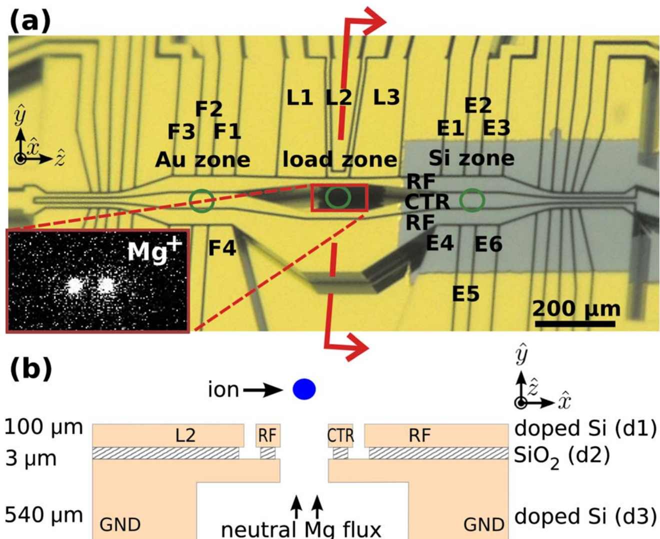

FIG. 2. (Color online) (a) Photograph of a multizone surface electrode ion trap fabricated from a single SOI wafer. Annotations highlight three trap zones (indicated by circles): a load zone (electrodes $L_1 - L_3$) and a pair of zones whose electrode surfaces were either bare silicon (electrodes $E_1 - E_6$) or 1 μm evaporated gold ($F_1 - F_6$, not all labels visible). Inset: Fluorescence from a pair of laser-cooled $^{24}Mg^+$ ion imaged onto a charge coupled device camera (viewed from above). (b) Chip geometry in cross-section near the loading zone; not to scale. The interelectrode spacing was $\sim$4 μm (e.g., between E_1 and E_2). The SiO_2 was undercut about $\sim$2 μm by a wet etch. A hole cut in layer d_3 permits passage of neutral ^{24}Mg from the back side of the wafer to the trap load zone without risk of shorting trap electrodes. The structural insulator (SiO_2) was outside the field of view of the ions in all zones.

the silicon and glass wafers were diced into chips and bonded. In this first demonstration device, the chips were aligned by hand with the aid of a microscope. The electrodes near the ions were bare silicon; the nearest glass surface was more than 2 mm away from the trap zone.

The rf potential $V_{RF}=125$ V at $\Omega_{RF}/2\pi=67$ MHz, was applied with a $\lambda/4$ resonant transformer with a loaded Q of 372. Typical ion lifetime with laser cooling was several hours; lifetime without laser cooling was up to 20 s.[11] The static trapping potentials were approximately $V(C_1)=V(C_1')=V(C_3)=V(C_3')=3$ V and $V(C_2)=V(C_2')=0$ V.

Figure 2 shows a trap with a surface-electrode geometry.[13,14] The substrate was commercially available SOI with a Si resistivity of 5 to 20×10^{-3} $\Omega\cdot$cm.[12] The single-layer geometry is amenable to microfabrication, as all the trap electrodes lie in a single plane. The trap has 45 electrodes, permitting translation of ions from a loading zone to a pair of arms each with multiple trapping zones. Near the end of each arm the electrodes taper so that the ion-electrode distance drops from $\sim$45 to 10 μm; these zones were not employed for the results reported here.

Trapping conditions were $V_{RF}=50$ V at $\Omega_{RF}/2\pi=67$ MHz and the rf resonant transformer loaded Q was 90. Typical ion lifetime with Doppler cooling was around an hour; without cooling the lifetime was 10 s. Trap potentials were determined numerically and designed to null ion rf micromotion and properly orient the trap principle axes.[10] Transport from the load zone to an experimental zone was repeated hundreds of times without ion loss (1 Hz repetition rate). The trap zone adjacent to electrodes E_2 and E_5 lies $\sim$371 μm away from the load zone and is $\sim$41 μm above the electrode surface. Typical static potentials were $V(E_1)=0.71$ V, $V(E_2)=-0.58$ V, $V(E_3)=0.20$ V, $V(E_4)=0.20$ V, $V(E_5)=-1.81$ V, $V(E_6)=0.71$ V, and $V(E_{CTR})=0.11$ V. For these potentials, the frequency along the $\hat{z}$-axis was measured to be $\omega_z/2\pi=1.125$ MHz, in agreement with simulation to within 4%. From simulation and measured radial frequencies ($\omega_x/2\pi=7.80$ MHz, $\omega_y/2\pi=9.25$ MHz), the rf potential was inferred. The trap depth predicted from simulation was 25 meV. Rf potentials as large as 150 V were applied to the devices; breakdown was not observed.

In the surface-electrode trap, kinetic energy gained by ions in the absence of cooling was measured by use of a Doppler recooling technique.[15,16] As a test of the effect of electrode material type on ion motional heating, the two following regions were created: one with gold-coated electrodes and one with bare silicon electrodes (Fig. 2). Heating measurements were made over each zone in a static potential well at an ion-electrode distance of $\sim$40 μm. We observed that ion motional heating in the absence of laser cooling[10] was the same in the gold and bare silicon experimental zones. The inferred electric field noise spectral density was competitive with other room temperature microtraps and was determined to be approximately 1×10^{-10} $(\mathrm{V/m})^2\cdot\mathrm{Hz}^{-1}$ at $\omega_z/2\pi=1.125$ MHz ($\sim20\times10^3$ quanta/s).[2,10,15,17] Because the rate of energy gain was about the same in both zones and somewhat variable from day to day, we suspect the heating was caused in part by noise injected from an unidentified external source.[9,12]

The two following types of Si-insulator-Si heterostructures were used for these traps: anodically bonded Si-glass-Si and commercial SOI. In both, trap electrodes were electrically isolated islands of conducting silicon formed by selective removal of material (Bosch DRIE). The etch pattern was defined by $\sim$7 μm photoresist. The narrowest practical channel width in a 200 μm wafer was 4 μm (50:1 aspect-ratio). Note that typical wet etch techniques for silicon (KOH, EDP) are ineffective in degenerate silicon.[18]

Two-tiered etching [Fig. 1(b)] was accomplished by use of a pair of overlapping etch masks and the additivity of the etch process. The lower mask was $\sim$1 μm thermal oxide and the top was $\sim$7 μm photoresist. After an initial deep etch, hydrogen fluoride (HF) was used to etch the exposed oxide, leaving the photoresist intact. A second deep etch completed the two-tier structure.[12]

Si-glass-Si heterostructures were assembled by use of anodic bonding.[18] In our experiments we fabricated structures with $d_1=100$ to 200 μm, $d_2=140$ to 200 μm, and $d_3=100$ to 600 μm. Anodic bonding of full wafers and individual chips was performed on a hotplate (450 °C and 500 V). Prior to bonding, chips were cleaned with HF and Piranha etch.

Through-wafer features were etched in the glass spacers before anodic bonding by ultrasonic milling. Alternately, it may be possible to etch the glass after bonding by use of silicon as a mask for a glass etchant such as HF. For $HF:H_2O=1:10$, the vertical etch rate is reported to be 10 μm/h with an undercut of 15 μm/h.[19]

Commercial SOI wafers are available with $d_1=0.1$ to 500 μm, $d_2=0.1$ to 10 μm, $d_3=100$ to 500 μm, and a resistivity as low as 0.5×10^{-3} $\Omega\cdot$cm, which helps reduce rf loss. For SOI, thermal silicon oxide usually forms the insulating layer (d_2).

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Ion trap chips were packaged in either co-fired ceramic chip carriers or planar ceramic circuit boards, both high vacuum compatible ($\sim 1 \times 10^{-9}$ Pa) and with gold traces.[20] The chips were adhered to the chip carriers by a ceramic paste. Ohmic contacts were deposited on the silicon chip (10 nm Al, 10 nm Ti, and 1000 nm Au). Native oxide was stripped by a plasma etch or HF dip before deposition of ohmic contacts and again immediately before inserting a finished chip into the trap vacuum system.

The $^{24}Mg^{+}$ ions were created by electron bombardment or resonant photoionization of thermally evaporated neutral magnesium atoms. The atom source was isotopically enriched ^{24}Mg packed inside a resistively heated stainless tube with an aperture pointing toward the trap loading zones. The ions were cooled to the Doppler limit by use of a laser tuned below the $^{24}Mg^{+}$ D2 transition at 280 nm.[12,15]

This letter presents approaches to building ion trap arrays that use degenerate silicon as an electrode material. Characteristics of two trap structures were presented and their performance suggests that this technology is compatible with trapping large arrays of ions for applications in QIP. The planar surface-electrode device demonstrated the feasibility of building monolithic ion traps in SOI. In addition to multizone traps, the goal of quantum computing could potentially be advanced by integration of these types of devices with CMOS electronics (e.g., via bump bonding), MEMS optics, and optical fibers.[6]

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